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Design of a High Efficiency DC-DC-Converter in Standard 180nm CMOS Technology.

ABSTRACT - Masterthesis

This works present the procedure to implement and design a dc-dc converter having a high efficiency for an input voltage from 4.5V to 36V with a maximum load current of 100 mA. The design is first implemented in the system level with the Verilog-A language, then it is carried on with the transistor circuit level. The converter has an operation mode for normal load condition, and another for small load current condition. The system can determine to use which mode automatically. The power train is a half-bridge circuit with a power PMOS transistor and a power NMOS transistor. The validation test bench also considered the existence of parasitic inductors in practice. In the normal load condition, the efficiency can reach to 97% at 8V output voltage with a load of 100 mA.