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Design and Verification of Handshake Protocols with QVL/OVL Checkers.

ABSTRACT - Masterthesis

This report presents a Master Thesis' work on the design and verification of hardware handshake protocols. Hardware handshake protocols are set of rules followed by hardware systems operating in different clock domains in order to communicate effectively and efficiently. As digital systems depend on clock signals for synchronisation, performance impairing issues attributed to large clock nets have been identified for complex systems. A few of these are power consumption, clock skew and generation of electromagnetic interference. One of numerous efforts made to eliminate this performance bottlenecks is in the adoption of Globally Asynchronous, Locally Synchronous Systems (GALS) to replace large synchronous systems design methodology. A key feature of GALS is segmentation of complex digital circuits into different smaller units with manageable local clock sizes. This methodology, however creates need for inter-unit communication capability within the system or between different systems hence the need for data exchange protocols, too. In response to these needs, a few standard protocols have been developed such as the I2C, SPI, UART, etc. This project therefore aims to understudy the basic architecture behind these protocols, design and verify three systems to demonstrate the basic handshake protocol architectures based on the phase change of the two control signals called “request” and “acknowledge”.