Faculty of Electrical Engineering & Computer Science
Master Degree Course Electronics Engineering, MSc EE

HSB
Hochschule Bremen
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Master 2021

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Circuit Design of Key Components for an ADC in Optical Communications.

ABSTRACT - Masterthesis

Advancing technology and mass usage of the internet-based/cloud-based services have led to increase in demand for the high-speed networks. The optical communication systems have evolved over the decades to be able to meet the demands of the high-speed networks. The optical receivers, which are an important part of the optical systems, are designed for high speed data transmission. They consist of parallelized ADCs, photodiodes, transimpedance amplifier and digital signal processor. The parallelized ADCs are the time interleaved ADC, which contains many ADC cores to reduce requirement for sampling clock and analog bandwidth.

This work is based on design and implementation of a 40 GS/s pipeline ADC with resolution of 6 bits. This ADC will be part of a time interleaved ADC with a sampling rate of 160 GS/s. The aim is to reach network speed of 1 Tb/s on a single wavelength in an optical receiver for high-speed data links.

For the design of this ADC, the medium resolution pipeline converter is implemented in the stages with 3-bit flash converters. The key components, such as comparators and encoders for the flash ADCs are designed using CML differential logic. The design is verified by simulations in time and frequency domain. Also, the power and area of the ADC is estimated....