Faculty of Electrical Engineering & Computer Science
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RISC V (PULP Version) Core Model Implementation in Synthesizable System C.

ABSTRACT - Masterthesis

This thesis shows the adaption of SystemC language to implement a RISC-V processor core based on the PULP microarchitecture, zero risky Figure 2.7. It is now possible to interact with SystemC language in different IDEs like COSIDE and VIVADO HLS. As well using software tools in linux as the standalone SystemC library and the RISC-V GNU tools. This document shows the obtained results during the development of the presented ideas in section 1.2 and as well shows the author's knowledge applied, acquired and refined during this time.

• A RISC-V processor core was implemented in SystemC, in COSIDE tool.

• The implemented model is able to execute a precompiled program, showing a valid functionality with the proposed testbench.

• The model was successfully migrated to VIVADO HLS, where the testbench was adapted with minor problems.

• About the synthesizeability of the model, it was possible to demonstrate, that the model is directly synthesizable, but not 100% successfully implemented after the synthesis.

• The reusability of the testbench was also demonstrated.