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Simulation Hardware Design and Verification of the Filter and Buffer Stages for an ADC and a DAC Board.

ABSTRACT - Masterthesis

The purpose of this thesis is to design filters and buffer stages for an ADC and a DAC circuits used for control and test systems. It is very common that a digital to analog converter (DAC) output is infested with glitches. The glitches are created mainly because of DAC output signal is switching from one level to another level, the switching mismatches of the major bit transition causes the significant glitches (e.g. the major glitches are created during the transition of binary code 1000 to 0111 or 0111 to 1000) in the DAC. There are several ways to deglitch the DAC output, in this thesis two approaches are implemented. First, is by utilizing sample and hold circuit. Second, is by using low pass filter, both of these approaches will be discussed in this thesis. A brief introduction about anti-aliasing filters is also given. Depending on different application purposes and to get the full-scale range of ADC, amplitude variation of analog input signal is needed. There are several methods to adjust the amplitude of analog input signal, among them are digital potentiometer with non-inverting operational amplifier and Programmable Gain Instrumentation Amplifier, both will be discussed in this thesis. In order to avoid the noise and other unexpected signal, which are generally created from analog signal sensors. An anti-aliasing filter is required to be placed in the input of the ADC. Implementing high speed buffer stages are also an important part of this thesis for both ADC and DAC. The most important part of this thesis is to design a 4-Layer PCB (Printed circuit board) with eagle software. Practical verification of the designed circuit is achieved as well in the laboratory by using experimental and printed circuit board, and results are found to be comparable to the theoretical ones.