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Master Degree Course Electronics Engineering, MSc EE

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Hochschule Bremen
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Master 2019

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Development of an Switched-Capacitor Programmable Gain Amplifier with Ultra-Low Power Consumption in Deep-Submicron SOI Technology.

ABSTRACT - Masterthesis

The aim of this work is development of a Switched-Capacitor (SC) Programmable Gain Amplifier (PGA) as an interface between sensors and an analog-to-digital converter (ADC). The designed block is a part of a long-life sensor front-end system. Therefore, the main challenge in this work is reduction of the average power consumption of the block below 5µW and satisfying the accuracy requirements. The PGA is needed for the system to handle with large dynamic range sensor signals. A switched capacitor implementation allows to avoid large static power consumption and to achieve accurate amplification. The project was done in 180nm SOI technology node.

During the project a fully-differential operational transconductance amplifier (OTA) was designed as the main building block of the PGA. Moreover, since the fully differential architecture requires common-mode feedback circuit (CMFB), a rail-to-rail differential difference amplifier (DDA) CMFB was designed. To size the circuits, algorithms based on gm/ID methodology were proposed. The algorithms were realized with MATLAB code and proposed in Appendix B.

The developed PGA was simulated with the help of Cadence Virtuoso. In addition to nominal DC, AC and transient simulations, the corner and Monte Carlo analysis were done. The results of the analyses show that maximum power consumption does not exceed 4.177 mW and all specifications are satisfied for nominal conditions. However, corner and Monte Carlo analyses revealed some problems associated with Slew Rate (SR) for some samples. The possible cause of the problem and its solution were proposed for the future work.