Faculty of Electrical Engineering & Computer Science
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Analyzing and Comparing Schematic and Layout Extracted Simulations of a Pipeline ADC-Design.

ABSTRACT - Masterthesis

This thesis describes comparison between the schematic and layout implementation of 10 bit pipeline ADC. The converter architecture is made up of nine stages with an inter stage gain of 2. The entire pipeline has been implemented in 22 nm CMOS FDSOI process using IIP nano sub modules from Fraunhofer IIS. IIP framework (IIP: Intelligent Intellectual Property) enables the automation of analog circuits in multiple design environments. IIP generators are parameterizable descriptions of each view of an analog block, i.e., layout, schematic and symbol. They allow the adaptation of complex layouts within seconds to minutes in order to incorporate hardly estimable parasitics and further considerations into the design flow. The given ADC design thus serves as a major test vehicle for IIP nano generator. The schematic design as such does not consider the parasitic capacitances and resistances. A physical layout considers all the non-idealities, thus the main focus was concentrated on analysing the performance degradation of the entire ADC going from schematic to layout by comparing the schematic simulation of the major sub modules with the extracted ones. Finally the comparison is done on the full layout of the pipeline ADC. The parameters describing the performance of the entire ADC were analyzed at the end and this helped in rating the performance of ADC as well as rating the performance of automatic layout generator as well. The simulations were carried out in Cadence environment using spectre simulator. This thesis also explores on understanding the design structures causing degradation in performance and also possibilities of improving them in the design. The work includes the results and discussions drawing conclusions from the simulation results in both schematic and layout levels.