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Development of a UVM testbench for SpaceWire IP cores.

ABSTRACT - Masterthesis

The present thesis approaches the UVM based verification of a freely available SpaceWire IP core. The aim is to develop a UVM testbench for those IP cores. The testbench shall be utilized for the automated verification of arbitrary SpaceWire IP cores, developed in conformity with the ECSS- E-ST-50-12C standard. In the theoretical part UVM basics required for the design are explained. Furthermore an explanation of the relevant contents of the SpaceWire standard is included. After that information about the SpaceWire Light IP core, which is utilized as a verified DUT as well as the basic testbench design concept is provided. The practical part begins with the description of the verification plan, developed based on a summary of the standard and which covers the behavior of the IP core. Finally, detailed explanations regarding the testbench development, from it's fundamental structure and the design of the agents and sequences to final tests and the verification of the IP core are given. The result of the thesis is a parameterizable UVM testbench for the verification of SpaceWire IP cores for which automated verification of the DUT still needs to be implemented.