Faculty of Electrical Engineering & Computer Science
Master Degree Course Electronics Engineering, MSc EE

HSB
Hochschule Bremen
City University of Applied Sciences

Master 2018

Debopam Ghosh

Design and Layout of a Channel Select Filter in 0.35 CMOS Technology.

ABSTRACT - Masterthesis

The aim of this thesis is to design and layout the chip level implementation of a channel select filter in 0.35 CMOS technology Channel select filters are used in receiver systems to tune to a particular frequency and eliminate the noise and the interference from the undesired channels with the aim of maximizing the Signal to Noise Ratio (SNR) at the receiver. The designed filter will be used along with a Low Noise Amplifier, which is used in microwave technology, for the purpose of reducing the noise.

There are two methods of channel selection in communication technology. The first is the super heterodyne concept where a local oscillator is used to tune the system's input RF frequency to the desired frequency. The second concept also involves the use of a local oscillator. But, the local oscillator's frequency in this case is very close to the receiving signal's frequency and hence is used to directly demodulate the incoming signal in the receiver. A channel selection filter is used in such a case to tune to the desired frequency. This channel select filter performs the function of a band-pass filter with precise frequency selection. The channel select filter is an active filter, implemented using a ladder network of operational amplifiers (opamp), resistors and capacitors.

The implementation will be done using Mentor Graphics analog/mixed signal IC tool chain in 0.35 CMOS technology. The design stages include behavioural modelling of the signal path using a mathematical analysis tool like MATLAB/Simulink and its validation, system level analysis and the final chip design along with area estimation of the created layout.