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Design of Low Pass Digital Impulse Response Filter for Frequency-Modulated Continuous Wave (FMCW) Radar Sensors.

ABSTRACT - Masterthesis

The automotive industries around the world are rapidly developing a variety of Advanced Driver Assistance Systems (ADAS). Using ADAS in the vehicle have proven to reduce road fatalities, by minimizing the human error. Few of the ADAS includes collision avoidance systems, adaptive cruise control, lane keeping, and parking assistance, which inform or actively support the driver to improve the critical task of driving a vehicle. ADAS relay on the camera, radar, LiDAR, ultrasonic, etc. to gather information about the vehicle surrounding, process the data and alert the driver or the modules in the vehicle for hazardous conditions. The system is expected to gather accurate input, be fast in processing data, accurately predict context, and react in real time. And it is required to be robust, reliable, and have low error rates.

In this thesis topic, a design of a robust system for processing the data gathered from radar frontend, used for distance measurement in parking assistance application has been presented. The system is implemented on the Zynq Ultrascale+ FPGA platform. At the beginning of the system, the analog signal from the sensor is converted to digital data using a high-speed ADC, which has a data rate of 40 MSPS. Next, the data rate of the system has to be reduced to an optimum value for an appropriate trade-off between accuracy and latency of the system using a decimator. Decimators essentially consists of a digital filter followed by down sampler. The digital filters in the DSP play a key role in determining the performance of the system. Hence, designing a suitable filter for the application is a very crucial part. This thesis work will present the design of FIR filter. Simulation results are used to study the behavior of the filters. Then, the best-suited filter will be implemented on the FPGA along with the other supporting blocks and the entire system is designed to run at an operating clock at 120 MHz.

The decimated data stored in the FPGA memory has to be transferred to a computer, where FFT can be performed and the distance information of the target can be obtained. To achieve this, the Gigabit Ethernet communication system has been designed for fast data transfers. In the end, the designed system is tested in the anechoic chamber to study the system's accuracy and stability.