Faculty of Electrical Engineering & Computer Science
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Modeling of a Delta-Sigma Modulator for a High Resolution Low Power Audio Frontend.

ABSTRACT - Masterthesis

This work describes an architectural study for delta-sigma modulators to be used in audio applications with medium performance at very low power consumption such as hearing aids. Higher order delta-sigma modulators prove to be the best candidates for such a requirement and hence they are analyzed in detail as part of this research work. The focus here is concentrated on a tradeoff between achievable resolution and noise floor versus power consumption. The comparison is concentrated on 3rd and 4th order modulators which also includes models for the decimation filters with necessary precision. A major part of the analysis involves MATLAB modelling and simulation which requires an initial system level study of these modulators. A Python package which is an equivalent of Richard Schreier's Delta Sigma Toolbox has been used for the same followed by Matlab Simulink®. Simulations from the Cadence Spectre environment have been used to obtain an approximation of the non-idealities introduced due to a 22 nm CMOS FDSOI process. The minimal requirements for performance parameters of the OTA has been determined through simulations which can significantly lower the power disspated since it acts as a major source of power dissipation in the ADC. The modulator post decimation and filtering achieves an SNDR of 102.7 dBc which results in an ENOB of 16.76 along with a THD of -134.3 dBc and hence provides a margin in the SNDR for process limitations and DAC noise floor.