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Methodology for Verification of Digital IPs within the Mixed-Signal Systems.

ABSTRACT - Masterthesis

Mixed-signal system complexity has evolved over time with increased demand for more complex functionalities and higher performance. An optimized system verification methodology is needed to ensure the correctness in the functionality of mixed-signal components. This thesis deals with the investigation of the verification approach of digital components in a mixed-signal environment and evaluation of such optimized system verification approach.

In this thesis, a multi-layer verification method and corresponding test bench are extended by implementing fixed-point model and a test bench in MATLAB for digital IP's verification. A fixed-point model implemented based on the existing floating-point model, is utilized and design is verified using MATLAB-HDL co-simulation. Further to improve the performance of the design, quantization effects in control loops are analyzed. This analysis involves an analytical approach to examine the behavior of the digital adaptive equalizer block of the system by reducing resolution. Minimum resolution to design the corresponding block is proposed, for which the quantization error remains below an acceptable limit. The developed verification methodology is used in the verification of the optimized design.

The proposed verification methods and models are exemplarily applied to an example 10BASE-T/100BASE-TX Ethernet PHY system which offers high-speed networking technologies for the interconnection of different elements within a spacecraft. This work utilizes the proposed verification methodology and results of the analysis to evaluate and analyze the possible deviations in implementation results versus specifications and provides the design guidelines on the optimal exploitation of the design space.