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Hardware Modeling and Verification of the MP3 Decoding Stage.

ABSTRACT - Masterthesis

Hardware Design appears to play important role for coming future not only because it acts as platform for any smart system but also because of these systems are spreading extensively in many fields of applications. These fields of applications are not limited to industry or manufacturing purposes but also individuals now start to use, for example, what is called single board computers to use it in their daily life activities. Therefore hardware design is important to be efficient in terms of its power consumption, area, cost, performance so that it can meet expected features at these end users. Another important requirement is to be able to use hardware components for performing different logic or arithmetic operations so that it can cover wide range of applications at end users. Building an MP3 decoder is a real practice for what is expected from hardware development process. It comprises complex arithmetic and logic operation that can be a sample of what any other application may demand to be hardware realized and it is clear how common is MP3 decoders in multimedia and communication systems. This was a motivation for starting this project which aims at hardware realization of the MP3 decoder.

This work discussed here is part of the hardware modeling of the MP3 decoder. Its scope is limited to the Decoding Stage which is a middle stage in the decoder responsible for decoding operations. i.e restoring original values of samples of the MP3 bit stream. Moreover, verification environment shall be created for this design also to emulate eventually how a hardware design process is carried out. Therefore this report is discussing initially important concepts regarding MP3 standards then starts with defining specifications of the design. Afterward comes implementation process of the design followed by how verification environment was created for this design. Obtained results are discussed at the end of this report.

Used Tools

Electronic Design Automation (EDA) tools are the tools that hardware engineers are using in all levels of design. This project is running in RTL level, therefore the following tools have been used .

- System Level Modeling: MATLAB.
- Design Abstraction: QuestaSim - HDL Designer, both are from Mentor Graphics.
- Simulation and Verification: QuestaSim.
- Synthesis: Xilinx ISE - Precision from Mentor Graphics.
- Auxiliary tools: Meld - Emacs.
- Hosting Platform: Linux Debian.