Faculty of Electrical Engineering & Computer Science
Master Degree Course Electronics Engineering, MSc EE

HSB
Hochschule Bremen
City University of Applied Sciences

Master 2016

Nanda Fathurrahman

UMV Testbench for a Floating Point Unit and Verification using Mentor Graphics Tools.

ABSTRACT - Masterthesis

Universal Verification Methodology (UVM) is the state-of-the-art methodology to enable efficient development and the reuse of verification environments throughout the digital chip industry, UVM is mostly applied by large teams of verification engineers, who are involved in the verification of highly complex system-on-chips, instead of modules of low to medium design complexity. To overcome difficulties in the application of UVM in the case of module level verification, there is a need to understand the particular benefits of UVM in such cases.

In this thesis two testbenches: The FPU Conventional SystemVerilog Testbench and the FPU UVM Testbench were developed and examined. This master thesis concludes that the FPU UVM Testbench offers more advantages that the other testbench implementation. It also demonstrated that Questa SIM verification management tools provides additional features to support the use of the UVM.