

**Master 2016**

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**Development of a fully automated CMOS Bandgap Voltage Reference IP for Multiple Technology Nodes down to 28 nm Automotive Applications.**

***ABSTRACT - Masterthesis***

Mixed-signal IC design for various technologies and design reuse is an issue for any company. One of the solutions is a bottom-up generator approach, which is a suitable way to realise a generic design. In this work, a hierarchical generator for on-chip voltage reference using the Intelligent IP library by Fraunhofer Institute is developed, which applied for two technologies -180 nm 28 nm. Additionally, the student has to analyse major layout effects, which should be considered regarding layout porting. The outcome of the master's thesis includes a tape out of the ready physical implementation of the design in two technologies.