Faculty of Electrical Engineering & Computer Science
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Metric Driven Mixed Signal Verification using UVM Power Management Unit.

ABSTRACT - Masterthesis

Mixed Signal Design Verification has been getting more importance from last few years. The reason being, in part, to the fact that todays mixed signal designs are complex in nature but richer in functionality, with efficient digital control units and configurations. The heterogeneous nature of the mixed signal design demands development of newer tools and productive methodologies for systematic and cost effective functional verification. The digital blocks of the design are represented using Register Transfer Level (RTL) and the analog blocks are either represented by behavioral models or transistor level net-lists. Therefore, close integration between analog and digital blocks makes functional verification challenging and there is a great need of improving the integration between digital and analog simulation environments.

This master thesis outlines a deterministic approach to design an effective functional verification test bench for stand-alone mixed signal module such as Power Management Unit (PMU). One of the important objectives of this project is to develop methods and systems to access quantities associated with an analog object such as Voltage, Current, Power or Op-Point parameter of a device. Modern approaches such as Metric Driven Verification (MDV) and Universal Verification Methodology (UVM) are used to maximize the verification effectiveness. The proposed verification methodology scales from a single IP block to a highly integrated system-on-chip (SoC), and is compatible with current digital-only verification methodologies, emphasizing the reusability of the test-benches.

This research work will also focus on creating a detailed test plan on mixed signal design block and explains the ways to manage this complex test cases using MDV. Cadence Incisive Enterprise Simulator is used to accomplish this project along with Infineon specific tools. The idea is to adopt the very methodology across the Infineon platforms in the future.