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**Development of an Analysis Tool for Equipment Productivity Losses
in Semiconductor Manufacturing.**

ABSTRACT - Masterthesis

It is a known fact that building and maintaining a semiconductor production fab has become increasingly expensive year by year and integrated circuit cost is going down year by year. To sustain this phenomenon and secure a permanent position in the global market, the global players have to reduce the cost by a minimum of 30% every year. The reduction of structure size which plays the main role in the technological progress leads to a cost reduction of 10-13% for each year. The increase of tool productivity and the increase of firm productivity contribute 15-18% to cost reduction approximately. This emphasizes the fact that increasing tool productivity has the major effect on cost reduction.

The productivity increase from a tool group directly influences the firm productivity, if these tools contribute to the bottleneck of the fab. The most expensive tools in the firm are considered as capacity bottleneck within the fabrication. As the cost of lithography tools almost amounts to one third of the total fab cost, they are considered as bottleneck. The increase in the efficiency of lithography tools leads to an increase in the capacity through which the cost reduction in the production line can be achieved.

To increase the lithography tools productivity, initially the productivity losses are to be identified from which potential areas can be achieved. This thesis has two fold. First part explains the manual analysis approach for finding the productivity losses in the lithography equipments. It also elucidates the productivity losses and the corresponding reasons for those losses through the manual analysis. There exist some limitations in manual analysis approach that demands for an automated process. Second part explains the automated algorithm approach in identifying productivity losses and improvement of the potentials in the photolithography equipments.