Faculty of Electrical Engineering & Computer Science
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Hardware Verification of I2C Protocoll using System Verilog.

ABSTRACT - Masterthesis

This thesis presents the design and Simulation of testbench to verify an I2C protocol. The design is described using the SystemVerilog® hardware description and hardware verification language. Initially I2C protocol was developed by Philips that was two wire mulimaster serial bus. I2C protocol is used for on board communication. Infrastructure of testbench is TLM-based that consists of stimuli generator, drivers, assertion module, scoreboard, coverage module and monitors. Verification runs using QuestaSim designed by Mentor Graphics. Verification is very important in the Chip design process. Unfortunately, verification effort is much less than designing effort that could cost a lot. This thesis is a humble effort to appreciate verification and to improve verification methods to face future challenges in chip designing.