Faculty of Electrical Engineering & Computer Science
Master Degree Course Electronics Engineering, MSc EE

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Design Methodology for Ultra-Low-Power CMOS Logic.

ABSTRACT - Masterthesis

The goal of this thesis is to develop a design methodology for Ultra-low power (ULP) CMOS logic for use in energy-autonomous sensor frontends.

To custom-design standard cell library is determined and implementation options for ULP CMOS logic gates for the library are investigated. A minimum set of ULP standard cells are designed, including schematic and layout, in a commercial 0.35 μm CMOS process, from which complex logic functions can be built. Cell characterization is done and the trade-off between power and speed are observed based on timing information extracted.

The designed cell library is used in creating digital functional blocks from Verilog descriptions. Thereafter, test designs are validated using cells from the reference library and the designed library. The trade-off for power vs. speed, area, library size is analyzed and conclusions are drawn based an the results obtained.