Faculty of Electrical Engineering & Computer Science
Master Degree Course Electronics Engineering, MSc EE

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High Speed Image Data Transfer from Host PC to Zynq-7020 via USB 3.0.

ABSTRACT - Masterthesis

In digital image processing, higher data transfer rates have become a prerequisite to attain major requirements of the customers. Also, it is equally important to process super speed data efficiently.

My research is an attempt to provide one such solution. The area of research is to interface high speed peripherals and process the data efficiently by interfacing USB 3.0 bus with Xilinx Soc(Zynq-7020).

Zynq-7020 is a combination of dual core ARM Cortex-A9 MPCore processor with seven series ARTIX FPGA on a single device or chip. Combination of both embedded processors and programmable logic provides an efficient processing platform. USB 3.0 super speed mode provides a transfer rate of 5 GB/s. Interfacing USB 3.0 and Zynq-7020 module provides a platform to transmit data at super speed and efficiently process the data at the same speed.

In order to provide USB 3.0 super speed functionality to Zynq-7020, Cypress USB 3.0 peripheral controller is employed. Primary goal of my research is to create an interface between USB 3.0 controller and Zynq-7020. Also, testing should be done to obtain the maximum throughput of this interface. Cypress USB 3.0 peripheral controller firmware needs to be programmed to interface with Zynq-7020. Cypress firmware is developed using 'C' language and developed using Cypress provided Eclipse IDE. Zynq-7020 is programmed by using Xilinx 14.3 (planahead tool, Embedded development kit and software development kit).