Faculty of Electrical Engineering & Computer Science
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Development and Analysis of a Library for Reliable and Energy Efficient Communication Elements for On-Chip Interconnects.

ABSTRACT - Masterthesis

Nowadays low power design is preferred; however it requires optimization at all levels. Therefore operation at the lowest possible voltage is highly desired. An approach in the deep-submicron era is to reduce the signal swing, in particular when driving long wires. The goal here is to develop a library of reliable, power-efficient circuits to drive low-swing signals. It includes, but is not limited to the analysis and investigation of the various on-chip driver and receiver circuit delays and energy efficiencies. Other aspects include reliability from noise analysis and statistical technology analysis namely, Monte-Carlo method. In addition, area of the components and layouts are included. Finally, comparisons at all levels are made to observe how the different circuit models performance changes for different design styles and operating conditions; verifying the functionality in different scenarios. Four different interconnect models are presented, explicitly a standard CMOS inverter, a basic Conventional-Level-Converter (CLC) and two more, known as the Differential (DIFF) and the Pseudo-differential (PDIFF). All circuits have their advantages and disadvantages that are practical for specific applications.

During the library development the technology used was TSCM65nm process and the software tools from Cadance Virtuoso. The design rules used for layouts were from Assura technology. This work has successfully completed a set of interconnect models with forthcoming applications for digital designers to be achieved. Nonetheless, future improvements regarding the layout and actual implementation are suggested.
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