Faculty of Electrical Engineering & Computer Science
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Verification and Validation of an Open Risk Processor on FPGA Platform

ABSTRACT - Masterthesis

Recent advancements in Field Programmable Gate Array (FPGA) technology have resulted in FPGA devices that realize the implementation of a complete embedded system an a single FPGA chip. The main and central component of any embedded system is processor. The softcore processors are like an ordinary microprocessor but are written in hardware descriptive languages. Those softcore processors can be synthesized and realized in any FPGA devices. In last past years, many FPGA vendors have provided the softcore processors to implement in the target FPGA technology.

In this thesis, OpenRISC 1200 processor is used which is 32-bit softcore processor and written in Verilog HDL. Xilinx ISE 12.4 is used to perform synthesize, design implementation and configure/program the FPGA. For verification and debugging purpose, a software tool chain from GNU is configured and installed. The software is written in C and Assembly languages. The communication between PC and FPGA board is performed through serial RS-232 port. The output can be seen at HyperTerminal on Windows XP. Fault injection methods are studied and emulation based method is applied to check the reliability and dependability of the system.

Today, FPGAs based softcore processor appear in a variety of embedded system devices, including industrial instruments, consumer electronics, automobiles, aircraft, copy machines, and application-specific computer hardware.