Department of Electrical Engineering & Computer Science
Master Degree Course Electronics Engineering, MSc EE

HOCHSCHULE BREMEN
UNIVERSITY OF APPLIED SCIENCES

Master 2005

Vijayakumar Kalyanaraman

Design of Architectures for the Implementation of Low-Power Digital Multi-Rate Filters

ABSTRACT - Masterthesis

Power dissipation has become a severe constraint on the physical level of a VLSI implementation due to increasing design complexity. For mobile systems, the maximum operating time between battery recharge depends on the power dissipation of the device. For high performance systems, the costs for heat removal and packaging due to significant power dissipation have become a major concern. At the same time, more and more parts of digital circuits are implemented using application specific instruction set processors (ASIPs). The subject of this thesis is the design of digital multi-rate filters in view of the reduction of the power dissipation.