Department of Electrical Engineering & Computer Science
Master Degree Course Electronics Engineering, MSc EE

HOCHSCHULE BREMEN
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Implementation of the GMC-TDD-XTDMA Mobile Radio Experimental System with VHDL Considering the Possible Complexity Reduction

ABSTRACT - Masterthesis

The thesis work is oriented towards implementing a Filter bank for Filtered Multi-Tone Modulation Technique (FMT) in Very High Speed Integrated Circuits Hardware

Description Language, commonly known as VHDL.

Chapter 1 describes the objective of the thesis work.

Chapter 2 deals with the basic fundamental blocks in a Filter bank.

Chapter 3 will describe the theory of Filter bank. A comparison is made between Orthogonal Frequency Division Modulation (OFDM) and Filtered Multi-Tone Modulation techniques which results in FMT as a better solution than OFDM for transmission. The practical implementation, i.e., efficient implementation is discussed also.

Chapter 4 is devoted to complexity reduction techniques and defines the final design constraints for the VHDL implementation.

Chapter 5 deals with VHDL implementation, synthesis and simulation. Chapter 7 describes the hardware setup and measurements results of the implementation.

Chapter 8 points down the outlook for the future work.